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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/760,741	01/17/2001	Jerry M. Brooks	M4065.0374/P374	5786

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EXAMINER	
CHU, CHRIS C	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 07/26/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/760,741	BROOKS, JERRY M.
	Examiner	Art Unit
	Chris C. Chu	2815

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 June 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1, 5 – 9, 11, 12, 15 – 21, 41 and 42* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1, 5 – 9, 11, 12, 15 – 21, 41 and 42* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. Applicant's amendment filed on June 21, 2004 has been received and entered in the case.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 5 – 9, 11, 12, 15 – 21, 41 and 42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ball (U.S. Pat. No. 5,291,061) in view of Wark (U.S. Pat. No. 5,696,031).

Regarding claim 1, Ball discloses in e.g., Fig. 1, Fig. 2 and column 2, lines 60 – 67 a semiconductor assembly comprising:

- a first semiconductor die (20) with a top and bottom surface;
- at least one second semiconductor die (18) having a perimeter, including four sides, and a top and bottom surface, said at least one second semiconductor die (18) being secured at its bottom surface to said top surface of said first semiconductor die by a flowable adhesive material (22, Since the thermoplastic-adhesive 22 is liquefied and hardened by heat repeatedly, the element 22 reads as flowable adhesive material

when the heat is applied) which does not extend past any one of the sides of said perimeter of said at least one second semiconductor die (since Fig. 1 does not show any adhesive material pasted or extended any one of the sides of a die 12, Ball discloses this limitation), said top surface of said first semiconductor die having at least one electrical contact area (under the wire 30N); and

- an encapsulating material (44) for encapsulating said at least one second semiconductor die, electrical communication, and at least a portion of said first semiconductor die, said encapsulating material filling a space between said bottom surface of said at least one second semiconductor die and said top surface of said first semiconductor die.

However, Ball does not disclose the location of the at least one electrical contact area on the top surface of said first semiconductor die being at a distance outside said perimeter of said at least one second semiconductor die, said bottom surface of the at least one second semiconductor die having a smaller area than said top surface of said first semiconductor die, and said at least one second semiconductor die being in electrical communication with said at least one electrical contact area on the first semiconductor die (claim 1). Wark teaches in e.g., Fig. 2 the location of the at least one electrical contact area (any pad on the die 26) on the top surface of said first semiconductor die (26) being at a distance outside said perimeter of said at least one second semiconductor die (32), a bottom surface of at least one second semiconductor die (32) having a smaller area than a top surface of a first semiconductor die (26), and the at least one second semiconductor die (32) being in electrical communication (a wire at the left-side that connects the die 32 and the die 26) with at least one electrical contact area (at the 3rd die pad from the left-

side of the die 26) on the first semiconductor die (26). Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Ball by using the location of the at least one electrical contact area, the bottom surface of the second semiconductor die to be smaller area than the top surface of the first semiconductor die, and the electrical communication between the first and second dice as taught by Wark. The ordinary artisan would have been motivated to modify Ball in the manner described above for at least the purpose of being accessible from above so that gold wire connections can be made to the lead extensions (column 1, lines 55 - 57).

Regarding claims 5 and 19, While Ball teaches the use of the adhesive material, Ball does not appear to provide any example of the adhesive's specific composition. Wark teaches in e.g., Fig. 2 the material of the flowable adhesive may be composed of an epoxy (28; column 5, lines 9 – 12). Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Ball by applying the epoxy as the specific material to form the adhesive material between the first and second dice of Ball as taught by Wark. The ordinary artisan would have been motivated to modify Ball in the manner described above for at least the purpose of reducing the manufacture cost by using the epoxy for the adhesive material.

Regarding claims 6 and 20, Ball discloses in e.g., Fig. 1, Fig. 2 and column 2, lines 60 – 67 said flowable adhesive material (16) covering an area less than or equal to "about" 90% of said at least one second semiconductor die bottom surface area.

Regarding claims 7 and 21, Ball discloses in e.g., Fig. 1, Fig. 2 and column 2, lines 60 – 67 said flowable adhesive material covering an area greater than or equal to "about" 50% of said at least one second semiconductor die bottom surface area.

Regarding claims 8 and 9, Ball discloses the claimed invention except for a distance between an electrical contact area and said perimeter of said at least one semiconductor die is less than or equal to about 200 microns. Since Wark shows in Fig. 2 an electrical contact area (any wiring pattern on the element 22) extends under the perimeter of a semiconductor die (26), Wark teaches the following limitation a "distance between an electrical contact area and a perimeter of at least one semiconductor die being less than or equal to *about* 200 microns". Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Ball by using the distance being less than or equal to about 200 microns as taught by Wark. The ordinary artisan would have been motivated to modify Ball in the manner described above for at least the purpose of diminishing circuit feature sizes and more power for the semiconductor device by packing chips on a small area (column 1, lines 48 – 55).

Regarding claim 11, Ball and Wark disclose said electrical communication being through a wire bond.

Regarding claim 12, Ball discloses in e.g., Fig. 1, Fig. 2 and column 2, lines 60 – 67 said at least one electrical contact area being a bonding pad (under the wire 30N).

Regarding claim 15, Ball discloses in e.g., Fig. 1, Fig. 2 and column 2, lines 60 – 67 a semiconductor assembly comprising:

- a first semiconductor die (20) having a top and a bottom surface;
- a second semiconductor die (18) having a perimeter, including four sides, and a top and bottom surface, said second die (18) being secured at its bottom surface to said top surface of said first semiconductor die by a flowable adhesive material (22) which does not extend past any one of the sides of said perimeter of said second

semiconductor die (see Fig. 1) such that there is a cavity along at least a portion of said perimeter between said first semiconductor die and said second semiconductor die (see Fig. 2);

- wherein said top surface of said first semiconductor die (18) has at least one electrical contact area (under the wire); and
- an encapsulating material (44) for encapsulating said at least one second semiconductor die, electrical communication, and at least a portion of said first semiconductor die, said encapsulating material filling said cavity.

However, Ball does not disclose the location of the at least one electrical contact area on the top surface of said first semiconductor die being at a distance outside said perimeter of said at least one second semiconductor die, said bottom surface of the at least one second semiconductor die having a smaller area than said top surface of said first semiconductor die, and said at least one second semiconductor die being in electrical communication with said at least one electrical contact area on the first semiconductor die, and a distance between an electrical contact area and said perimeter of said at least one semiconductor die is less than or equal to about 428 microns (claim 15). Since Wark shows in Fig. 2 an electrical contact area (any wiring pattern on the element 22) extends under the perimeter of a semiconductor die (26), Wark teaches the following limitation a "distance between an electrical contact area and a perimeter of at least one semiconductor die being less than or equal to *about* 428 microns". Also, Wark teaches in e.g., Fig. 2 the location of the at least one electrical contact area (any pad on the die 26) on the top surface of said first semiconductor die (26) being at a distance outside said perimeter of said at least one second semiconductor die (32), a bottom surface of at least one second semiconductor

die (32) having a smaller area than a top surface of a first semiconductor die (26), and the at least one second semiconductor die (32) being in electrical communication (a wire at the left-side that connects the die 32 and the die 26) with at least one electrical contact area (at the 3rd die pad from the left-side of the die 26) on the first semiconductor die (26). Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Ball by using the smaller die for the second die, the location of the electrical contact area being at exterior to said perimeter of said second semiconductor die, the electrical communication between the first and second dice, the distance being less than or equal to about 428 microns as taught by Wark. The ordinary artisan would have been motivated to modify Ball in the manner described above for at least the purpose of diminishing circuit feature sizes and more power for the semiconductor device by packing chips on a small area (column 1, lines 48 – 55).

Regarding claim 16, Ball discloses in e.g., Fig. 2 said first semiconductor die (20) being secured to a support structure (14, 28A and 28N).

Regarding claim 17, Ball discloses in e.g., Fig. 2 said support structure (14, 28A and 28N) being a film.

Regarding claim 18, Furthermore, While Ball teaches the use of the support structure, Ball does not appear to provide any example of the support structure being a printed circuit board. Wark teaches in e.g., Fig. 2 the support structure being a printed circuit board (22; column 4, lines 3 - 22). Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to further modify Ball by using the PCB for the support structure in the place of the support structure of Ball as taught by Wark. The ordinary artisan would have

been motivated to modify Ball in the manner described above for at least the purpose of diminishing the thermal shock between the support structure and the semiconductor device.

Regarding claims 41 and 42, Ball discloses in e.g., Fig. 1, Fig. 2 and column 2, lines 60 – 67 a semiconductor assembly comprising:

- a support structure (14, 28A and 28B) having a top surface; and
- at least one first semiconductor die (20) having a perimeter, including four sides, and a top and bottom surface, said bottom surface having a smaller area than said top surface of said support structure (see Figs. 1 and 2), said at least one first semiconductor die (20) being secured at its bottom surface to said top surface of said support structure by a compressed flowable adhesive material (24; Since the element 24 is same as the element 22 and the thermoplastic-adhesive 22 is liquefied and hardened by heat repeatedly, the elements 22 and 24 read as flowable adhesive material when the heat is applied) which does not extend past any one of the sides of said perimeter of said at least one semiconductor die (since Fig. 1 does not show any adhesive material pasted or extended any one of the sides of a die 12, Ball discloses this limitation), said compressed flowable adhesive material covering an area greater than or equal to "about" 50% of said at least one semiconductor die's bottom surface area (claim 42; see Fig. 2), such that there is a first cavity (a gap between the element 20 and the element 14) along at least a portion of said perimeter between said support structure and said first semiconductor die, said first cavity being filled with an encapsulating material (44) such that only said adhesive material and said encapsulating material are between said first semiconductor die and said support

structure, said top surface of said support structure having at least one electrical contact area (at the area under the reference number 36) at a distance outside said perimeter of said at least one semiconductor die, said at least one semiconductor die being in electrical communication (30N) with said at least one electrical contact area; and

- a second semiconductor die (18) having a perimeter, including four sides, and a top and bottom surface, said second semiconductor die being secured at its bottom surface to said top surface of said first semiconductor die by a compressed flowable adhesive material (22, Since the thermoplastic-adhesive 22 is liquefied and hardened by heat repeatedly, the element 22 reads as flowable adhesive material when the heat is applied) which does not extend past any one of the sides of said perimeter of said second semiconductor die (see Fig. 1) such that there is a second cavity along at least a portion of said perimeter between said first semiconductor die and said second semiconductor die, said second cavity being filled with said encapsulating material (44; see Fig. 2).

However, Ball does not disclose said bottom surface of the second semiconductor die having a smaller area than said top surface of said first semiconductor die. Wark teaches in e.g., Fig. 2 a bottom surface of a second semiconductor die (32) having a smaller area than a top surface of a first semiconductor die (26). Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Ball by using the bottom surface of the second semiconductor die to be smaller area than the top surface of the first semiconductor die as taught by Wark. The ordinary artisan would have been motivated to modify

Ball in the manner described above for at least the purpose of stacking multiple dice on top of the wire-bondable IC die (column 5, lines 22 – 23).

Response to Arguments

4. Applicant's arguments with respect to claims 1, 15, 41 and 42 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chris C. Chu whose telephone number is 571-272-1724. The examiner can normally be reached on 11:30 - 8:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 517-272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov.

Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chris C. Chu
Examiner
Art Unit 2815

c.c.
7/19/04 6:43:57 PM

Tom Thomas

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